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A Review of Machine Learning Techniques for Analog Integrated Circuit Design and Optimization

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ABSTRACT: Analog electronic design automation has historically lagged behind its digital counterpart due to the complex, multi-dimensional design space and strict sensitivity to parasitic effects, process variations, and geometric constraints. A comprehensive review of the evolution, current state-of-the-art, and future trajectories of electronic design automation tools specifically tailored for analog integrated circuit design could serve as a foundational roadmap for researchers and tool developers working to bridge the automation gap between analog and digital integrated circuit design. The present article does a state-of-the-art review from three perspectives; in a first phase, a review of algorithms present in the electronic design automation field is performed, highlighting use frequency, strengths and limitations of the more popular algorithms. Afterwards, it categorizes and evaluates recent advancements across several design phases: circuit sizing and optimization, automated topology generation, circuit verification, and physical layout generation (placement and routing). Special emphasis is placed on the paradigm shift from traditional, heuristics-based optimization to modern machine learning and deep reinforcement learning techniques, which have drastically reduced computational overhead while maintaining high optimization accuracy. Furthermore, this article addresses advances from the perspective of application use cases, presenting the progress that has been achieved with different circuit use cases, such as operational amplifiers, low dropout regulators, or voltage references. Finally, this review highlights open research directions, emphasizing the need for standardized benchmarks and robust, artificial intelligence-driven frameworks capable of seamless integration into existing commercial design flows.

KEYWORDS: analog circuit design, circuit sizing, topology optimization, Bayesian optimization, machine learning, neural networks, reinforcement learning, evolutionary algorithms, operational amplifiers, oscillators, low dropout regulators

1. Introduction

Analog and mixed-signal design remains one of the most effort-intensive stages of the integrated-circuit development cycle. Performance is sensitive to process, voltage and temperature variation and to device mismatch, and the specifications of interest must typically be satisfied simultaneously rather than traded off one at a time. Sizing and topology decisions are therefore still largely made by hand, guided by designer expertise, and much of that effort must be repeated at every migration to a new technology node. Machine learning has consequently become an essential part of several stages of the integrated-circuit design cycle. Regression and surrogate models replace costly simulation in circuit sizing [1, 2]; population-based and learning-guided search address topology selection and device-level optimization as constrained extremum-search problems [3, 4]; machine learning-based approaches support pre-silicon verification [5, 6]; and layout-oriented methods have been used for routing, well generation and post-layout performance prediction [7, 8].

Early efforts to automate analog integrated-circuit design grew out of attempts to encode expert design knowledge and heuristic reasoning into computer aided design (CAD) frameworks. Interactive, knowledge-based tools such as IDAC [9], OASYS [10], and STAIC [11] represented circuit topologies and sizing procedures as hierarchies of design templates or dependency structures, allowing established design expertise to be captured and reused across performance specifications. DELIGHT.SPICE [12] coupled gradient-based and controlled-random-search algorithms directly to circuit simulation. OPASYN [13] then merged heuristic topology selection with analytic-model-based parametric optimization to compile CMOS operational amplifiers automatically, illustrating how heuristic and optimization-based reasoning could coexist within a single synthesis flow. As these frameworks matured, explicit artificial-intelligence techniques were introduced to capture the qualitative judgment central to analog expertise. The two-part ISAID system [14, 15] applied qualitative reasoning to both generate initial topologies and automatically correct designs violating specifications, while FASY [16] introduced fuzzy-logic-based topology selection whose decision rules could be generated automatically through a learning process driven by an internal optimizer, an early

instance of rule induction from optimization experience within analog CAD. Concurrently, biologically inspired search emerged as an alternative to gradient- and rule-based methods: SEAS [17] adapted simulated-evolution concepts to explore non-fixed topologies, while DARWIN [18] applied a genetic algorithm to jointly evolve operational amplifier topology and transistor sizing.

These knowledge-based and optimization-driven frameworks relied on hand-crafted rules and analytic models that became increasingly difficult to maintain as technology scaled and circuit behavior grew more nonlinear. As transistor-level simulation data and computing power became more abundant, it grew more practical to learn design relationships from data rather than encode them explicitly. This shift redirected research from rule induction and simulated evolution toward neural-network-based modeling, surrogate-assisted optimization, and, more recently, reinforcement-learning and graph-neural-network approaches that generalize across topologies and technologies with less manual effort.

In recent times, the trajectory of analog IC electronic design automation reflects a steady shift from encoding human expertise toward learning it directly from the design problem itself. Early research relied on expert system implementations, in which designers manually distilled their knowledge into explicit rules, heuristics, and decision trees; these systems were transparent and fast but brittle, difficult to maintain, and unable to generalize beyond the topologies and specifications their creators had anticipated.

To escape this dependence on hand-crafted knowledge, the field turned to metaheuristic optimization, most notably genetic algorithms (GA), which treat sizing as a global search problem and evolve populations of candidate circuits against simulator feedback, gaining flexibility at the cost of many expensive simulations. Bayesian optimization (BO) addressed this inefficiency by building a probabilistic surrogate of the performance landscape, enabling far more sample-efficient exploration by reasoning about where the next evaluation is most informative. Reinforcement learning (RL) then framed design as sequential decision-making, training an agent to learn a reusable sizing or topology policy through repeated interaction with the simulator, so that experience could transfer across problems rather than being discarded after each run.

Most recently, large language model (LLM) approaches push this arc further by combining the interpretability of the original expert systems with the adaptive side of learning-based methods: LLM agents can ingest design specifications in natural language, reason over prior knowledge, invoke optimization and simulation tools, as the previously mentioned BO/GA/RL-based frameworks, and coordinate the overall workflow, effectively acting as automated design experts that coordinate the optimization and learning techniques that preceded them.

The remainder of this article is organized as follows. Section 2 presents a comparative analysis of the machine learning algorithms reported in the literature, identifying the methodological trends and the preferences that have emerged across the surveyed corpus.

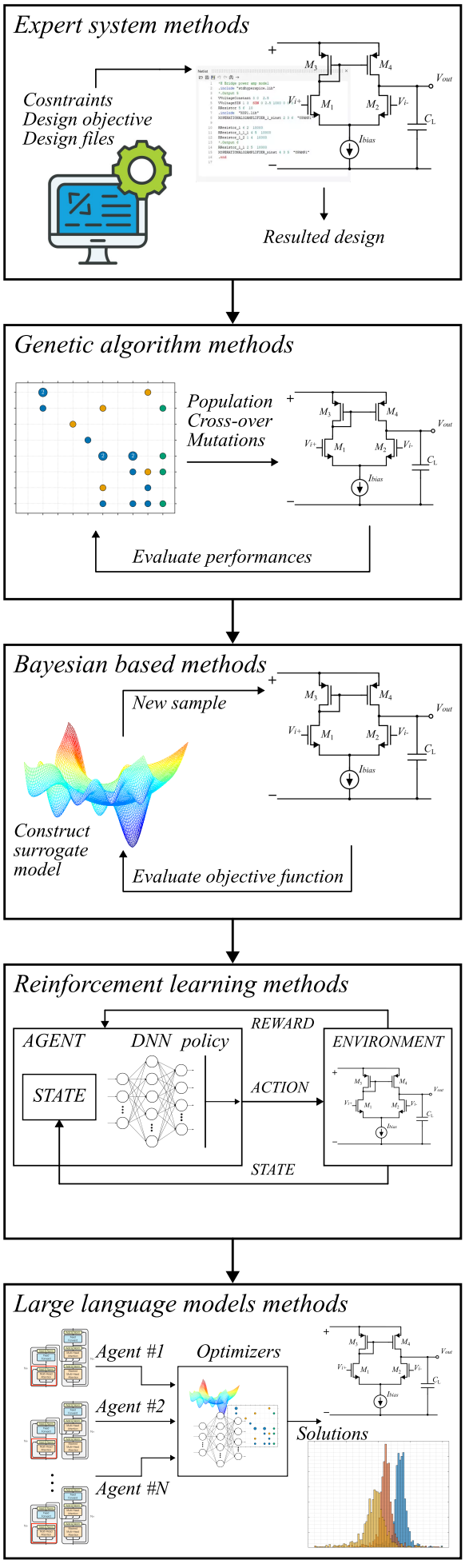


Figure 1: Evolution of ML trend algorithms in EDA

Section 3 adopts a application-centered perspective, examining which design problems have been advanced most substantially, which use cases have proven most amenable to automation, and which remain comparatively underrepresented. Section 4 draws the two perspectives together, comparing recurring algorithm and circuit-level approaches in terms of reported performance. Section 5 concludes the article and outlines directions for future work.

2. A comparative analysis of machine learning algorithms popular in electronic design automation

To begin the review of state-of-the-art, an analysis regarding the used algorithms has been done. This analysis is presented in Figure 2. Over the selected literature review, comprising a consistent amount of papers, a majority contain artificial neural networks (ANNs) [19] used in different tasks (sizing, optimization, black-box modeling, etc.). Several reasons can be attributed to this preference, namely the ease of implementation, robustness and flexibility with bigger data sets. Close to the ANNs we can observe Genetic Algorithms (GAs) [20] and Bayesian Optimization (BO) [21] approaches to be favorable for applications and in the fourth position reinforcement learning (RL) [22]. Recently, large language models (LLMs) based approaches such as [23, 24, 25] have gained a lot of interest (as presented in Figure 3). There is a growing interest in LLMs and it could be expected this type of approach to break through into the top positions, potentially surpassing BO and GA as the preferred algorithms.

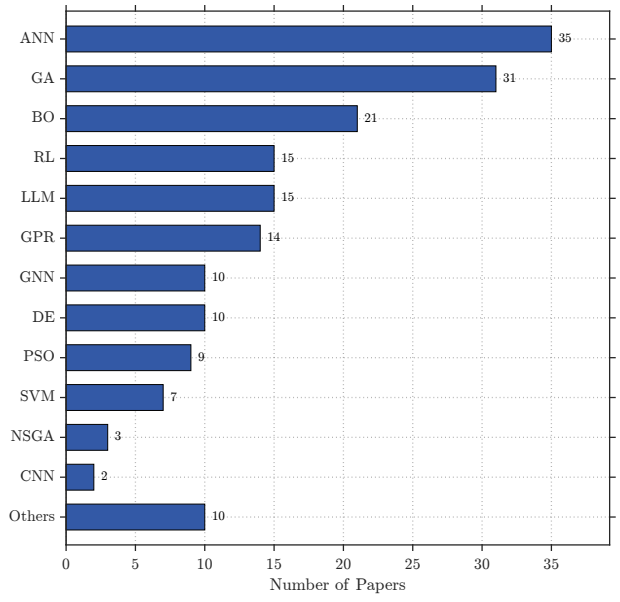


Figure 2: Frequency of different ML algorithms used in literature

On the lower half of the graph we see a series of regression and optimization algorithms which are secondary in the field but with respectable results nonetheless. Gaussian process regression (GPR) [26], Graph neural networks (GNNs) and cellular neural networks (CNNs) and Support vector machines (SVM) are among the lesser preferred regression algorithms, and for optimization approaches we mention differential evolution (DE) and particle swarm optimization (PSO).

Each of the frequently reported algorithms is then examined in a dedicated subsection. For every algorithm category we consider the design tasks to which it has been applied, the way the design problem is formulated, the performance reported against the benchmarks used, and a short introduction to each algorithm presented.

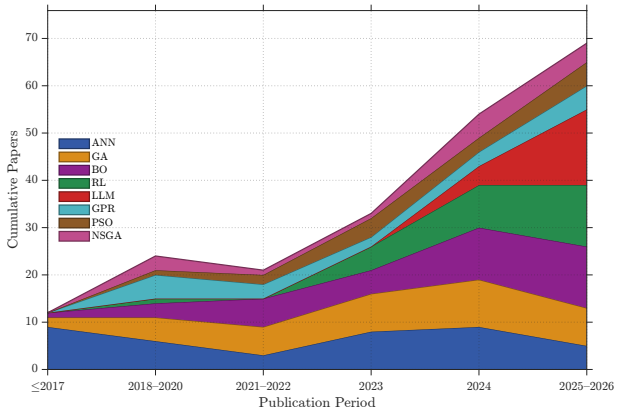


Figure 3: The trend of different ML algorithms over time.

2.1. Neural networks based approaches

Neural networks [19] are a popular choice used in electronic design automation (EDA) to rapidly predict performance metrics like power consumption, area and circuit behavior drastically accelerating complex chip design that would otherwise take hours or days using traditional simulation tools. The input-output relationship of a multilayer perceptron (MLP) artificial neural network can be expressed as:

$$f(\mathbf{x}) = \sum_{i=1}^{m} \alpha_i \tanh(\mathbf{W}^T \mathbf{x} + \mathbf{b}) \tag{1}$$

where the input is a vector of n variables (features) $\mathbf{x} \in \mathbb{R}^n$ with $\mathbf{x} = [x_1, x_2, \ldots, x_n]$ and the output is a scalar variable $F(x) \in \mathbb{R}$. α_i are the output weights that connect the hidden layer to the output and $\mathbf{b} \in \mathbb{R}^m$ is the bias vector. The matrix $\mathbf{W} = [\mathbf{w}_1 \ldots \mathbf{w}_m]$ is an n-by-m matrix that connects the inputs to the hidden layer of m neurons characterized by a hyperbolic tangent function as the activation function.

The main property of ANNs of the form in (1) is that they are universal approximators, being capable of modeling any continuously unknown function which can be differentiated over a given interval. The process of adjusting the network free parameters W, α, b in order approximate a function $f(\mathbf{x})$ is commonly referred to as the training procedure. Thus, for training the ANN we use a set of M data point pairs $\mathbf{x} = [\mathbf{x}_1 \ldots \mathbf{x}_M]$ and $y = [1 \ldots\ldots y_M]$ generated by the unknown function $f(\mathbf{x})$ (simulator/circuit in the presented cases) as:

$$y = f(\mathbf{x})$$

Neural network-based methods have become a mainstream tool for automating several stages of analog and

mixed-signal IC design [27]. The earliest and most persistent application is transistor-level sizing: feedforward and generalized regression networks were first used to size fundamental blocks such as current mirrors and differential amplifiers in a technology-independent manner in [28]. The same approach was later extended to two-stage operational amplifiers (OAs) [2, 29] and more general forms of amplifier topologies [30, 31] and lastly filter design in [32]. In these reports, the ANN was used as a *pseudo-designer* meaning that performances (P) were used as inputs and design parameters (DP) of the circuits physical properties were the predicted outputs of the ANN. DP can consist of transistor widths and lengths, resistances, capacitances and bias currents or voltages and subsequently performances can be any measured performance of the circuit, such as gain, bandwidth, power consumed, etc. A general example of this is depicted in Figure 4. In [33], this approach is used to size a two-stage OA and in [34] a similar approach using deep neural networks (DNNs) and recurrent neural networks (RNNs) are used to size a similar two-stage OA as a use case.

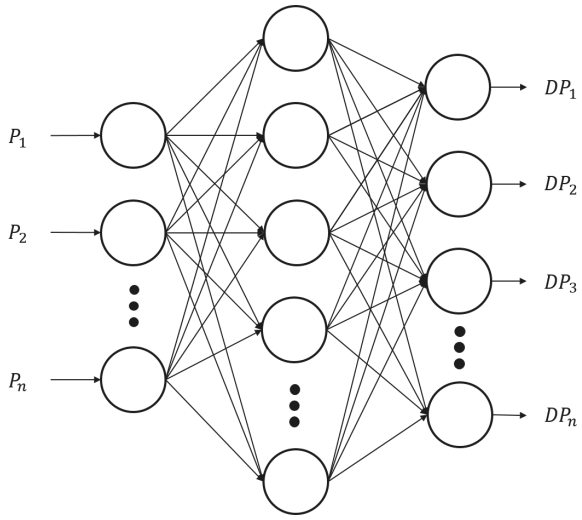


Figure 4: Block diagram of a NN in pseudo designer

Alternatively the ANN can be trained with the design parameters (DP) as inputs and as outputs the performances (P). This mode of operation is conventionally named *pseudo-simulator* (Figure 5) since the ANN is used as a placeholder for simulator use [35]. This distinction is further explained in [36].

The *pseudo-simulator* approach can be easily coupled with a ML optimizer as in [37] where the sizing was subsequently accelerated by replacing SPICE evaluations with ANN surrogates inside evolutionary algorithms or particle-swarm optimization, and also by chaining polynomial regression with ANNs for sizing reuse [1], and by combining ANN with genetic algorithms for design-space exploration in [35].

Neural networks have also become the dominant machine learning technique across the analog/RF EDA flow, with several recurring aims. Some of the aims of ML models are simulation runtime reduction, performance optimization, and power reduction. In [38], authors propose an automatic simulation-based sizing approach which is essential in designing radio-frequency (RF) voltage-controlled oscillators (VCO), and in [39] deep-learning loops were used to automate power-amplifier optimization. A related line of work coupled ANN regression with VAE-based candidate verification for VCO sizing [40]. Specialized applications are also present, including ANN-based fault diagnosis and constrained parameter extraction for RF amplifiers [41] and machine-learning paradigms for post-silicon debug of RF/analog circuits [42]. A comprehensive study for of ANN structures for microwave CAD covering filters, oscillators, and transistor modeling is presented in [43].

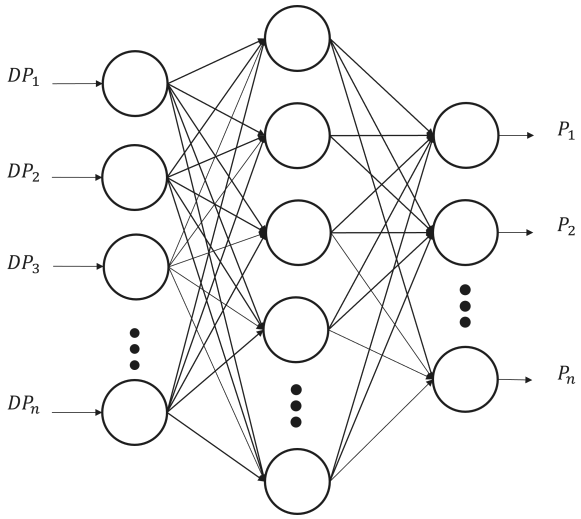


Figure 5: Block diagram of a NN in pseudo simulator

Several circuits where optimized with the use of a cascaded NNs approach together with GAs [44] and [45]. The authors report favorable results for VCO, low noise amplifier (LNA) and a mixer in [44] and several OA topologies in [45]. Similarly, in [46] authors used ANN-based regression coupled with GAs to optimize OA performances with the g_m/I_D method of sizing. The versatility of ANN-based sizing is shown in [47], where authors report high accuracy sizing for amplifiers and low dropout regulators (LDOs).

At the system level, ANN classifiers and regression networks have been used to select modulator topologies and directly infer high-level design variables for Sigma-Delta modulators with reported > 60× CPU-time savings in [48]. In a further publication, a mixed approach with simulated annealing to cuts power consumption by roughly 38% [49]. Beyond sizing, ANNs have enabled full topology generation and synthesis, as in the semi-supervised co-learning framework AnGeL [50], which reduces labeled-data requirements by over three orders of magnitude.

Simulation and macromodeling acceleration is another major thread: in [51] ANN models converted to Verilog-A achieve 5× speed-ups for operational transconductance amplifiers (OTAs) design when compared to simulating it at the transistor level. In [52] a reusable machine-learning macro-models of linear ICs and ADC/DACs reach 3600× speedup over SPICE with sub-1% error in modeling. To improve the data acquisition process in [53] an active-learning sampling scheme that reduce the training data needed for accurate LDO behavioral metamodels is presented. In [54] recurrent neural networks (RNNs) are introduced as an

alternative to ANN modeling for high-speed nonlinear circuits.

2.2. Evolutionary algorithms based design

Genetic algorithms [20] are a particular class of evolutionary algorithms that use techniques inspired by evolutionary biology such as inheritance, mutation, selection, and crossover. Figure 6 shows a graphical representation of the genetic algorithm mechanisms in the IC design context. A more detailed mathematical description of evolutionary algorithms is presented in [20] which the reader can further explore.

Genetic algorithms involve a search from a population of individuals. In the initialization of a genetic algorithm population, each individual is randomly generated. Each individual is evaluated according to a fitness function which aims to maximize certain aspects of the population. Each iteration will preserve the elite individuals and the rest of the population will be new individuals generated by the mutation and crossover mechanism. The algorithm will continue to generate new individuals until the stopping condition is met, which can be a certain population size or a certain individual that meets all the imposed stopping criteria. This process makes genetic algorithm well suited to combinatorial and continuous problems.

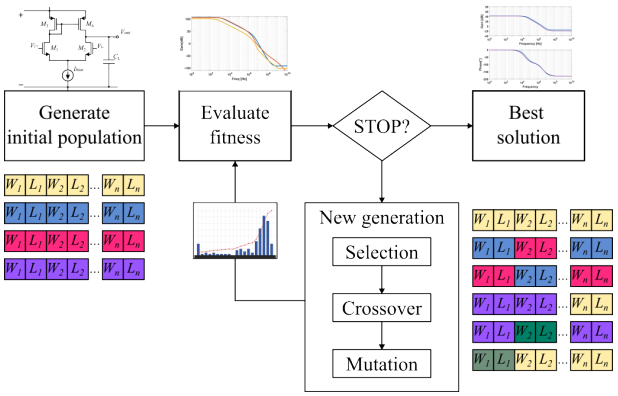


Figure 6: Block diagram of a genetic algorithm

In the context of IC sizing and optimization, genes of the algorithm are represented by physical and electrical characteristics of the circuits, such as transistor widths and lengths, resistors, capacitors, or bias voltages and currents. Design objectives are comprised of any measurable outputs from the circuits such as output voltages and currents, bandwidths or power consumption.

Evolutionary algorithms (EAs) have become a mainstay of electronic design automation (EDA), particularly for analog and mixed-signal integrated circuits, whose non-convex, experience-driven design spaces resist gradient-based methods. Recent reviews position genetic algorithms (GAs), alongside particle swarm optimization and reinforcement learning, as important algorithms spanning topology synthesis, parameter optimization, and transfer learning, while framing the analog-specific drivers of non-linearity, PVT sensitivity, and conflicting objectives [55, 56].

Regarding circuit optimization, several publications report various OA topologies as use cases. In [57, 58] and [59], the utility of GAs for automating electronic design using multi-objective genetic algorithms is demonstrated, jointly optimizing gain, bandwidth, phase margin, slew rate, area, and power. In [60], a similar approach was reported which combines GAs with g_m/I_D method used for sizing several OA circuits, also taking into account PVT variations. A simulation-efficient approach is reported in [61], where for the same simulation budget a 46% greater figure of merit compared to other methods is reported. Beyond amplifiers, GA-driven frameworks size charge-pump circuits to sub-2% specification error [62] and comparators through GA topology choice coupled to SPICE parameter tuning [63].

In [3], authors introduce MODEBI, a Gaussian-process surrogate model which preselects differential-evolution candidates for LDO sizing is presented and in [64] a corner-aware strategy is further developed based on the initial study. A similar surrogate model-assisted evolutionary algorithm approach is presented in [65] with results on OAs and VCOs.

Another important use case is topology synthesis (performance optimization without a fixed structure). In [66], authors introduce PSADE for automated synthesis of analog circuit topologies, based on an evolutionary algorithm. In [67], a circuit synthesis tool is presented; the approach accomplished synthesis of different amplifiers without any prior knowledge of predefined topologies.

EA-inspired approaches such as particle swarm optimization (PSO) [68] , and cuckoo search algorithms [69] have been successfully used in circuit sizing. Other DE-based approach have found success in circuit sizing, such as [70] multi-objective DE approach that cuts simulations by up to 63% while surpassing expert manual designs, and also a PSO-DE hybrid approach [71] which obtained better results than traditional PSO and DE approaches. ESSAB [72] combined DE with ANN surrogates and a novel candidate-ranking scheme to size amplifiers and a comparator under complete sets of stringent specifications. Lastly, [73] introduces a mixed approach between EAs and BO.

2.3. Bayesian optimization based approaches

Bayesian optimization (BO) [21, 26] has emerged as the dominant sample-efficient paradigm for simulator-in-the-loop analog sizing. Several publications, report successful implementation of various BO-based approaches [74, 75, 76, 77, 78, 79] with significant improvements such as significant simulation cost reduction and improvement of overall design. An intuitive graphical explanation is provided also in Figure 7.

At its core, Bayesian Optimization (BO) is formulated to find the global maximizer of an unknown, computationally expensive, and potentially noisy black-box objective function $f(x)$:

$$x^* = \arg\max_{x \in \mathcal{X}} f(x) \tag{2}$$

where $\mathcal{X} \subset \mathbb{R}^d$ is the bounded domain of interest. Since

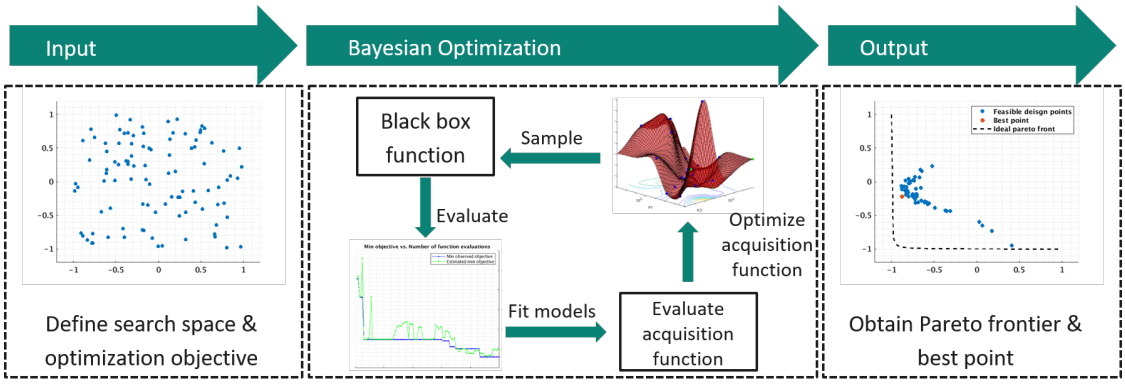


Figure 7: Bayesian optimization principle.

evaluating $f(x)$ directly is highly expensive, we model our belief about the objective function using a probabilistic surrogate model. The most widely used model is a Gaussian Process (GP) [26], which acts as a prior over functions:

$$f(x) \sim \mathcal{GP}\left(m(x), k(x, x')\right) \tag{3}$$

where $m(x)$ is the mean function, often assumed to be zero or a constant for simplicity and $k(x, x')$ is the covariance function (or kernel), which encodes the prior assumptions. Given the dataset $\mathcal{D}_{1:t}$ and observations y_i defined as:

$$\mathcal{D}_{1:t} = \{(x_i, y_i)\}_{i=1}^{t} \tag{4}$$

$$y_i = f(x_i) + \varepsilon_i \tag{5}$$

which are subject to independent Gaussian noise $\varepsilon_i \sim \mathcal{N}(0, \sigma_n^2)$, the conditioned posterior distribution of the function at a new candidate point x is Gaussian:

$$f(x) \mid \mathcal{D}_{1:t} \sim \mathcal{N}\left(\mu_t(x), \sigma_t^2(x)\right) \tag{6}$$

The analytical expressions for the posterior mean $\mu_t(x)$ and variance $\sigma_t^2(x)$ are given by:

$$\mu_t(x) = \mathbf{k}(x)^T \left(\mathbf{K} + \sigma_n^2 \mathbf{I}\right)^{-1} \mathbf{y}_{1:t} \tag{7}$$

$$\sigma_t^2(x) = k(x, x) - \mathbf{k}(x)^T \left(\mathbf{K} + \sigma_n^2 \mathbf{I}\right)^{-1} \mathbf{k}(x) \tag{8}$$

An acquisition function $\alpha(x; \mathcal{D}_{1:t})$ is an utility metric calculated from the GP posterior. It quantifies the value of selecting x as the next sampling candidate. We determine the next query point x_{t+1} by solving:

$$x_{t+1} = \arg\max_{x \in X} \alpha(x; \mathcal{D}_{1:t}) \tag{9}$$

In [74, 75, 76, 77, 78, 79], several BO optimization approaches are proposed for optimization of analog IC. As use cases, OAs are present almost ubiquitously, together with other related circuits such as power amplifiers (PAs) [74, 75], voltage-controlled oscillators (VCOs) [76, 78], low-noise amplifiers (LNAs) [77, 80], charge-pumps [78], and lastly, low dropout regulator (LDO) and bandgap voltage reference (BGR) are presented in [79].

The mentioned papers attempt to overcome three recurring bottlenecks: GP scalability, the issue of high dimensionality, and process variation. Scalability has been addressed by replacing the exact GP with sparse pseudo-input approximations that reduce training and prediction to $O(N)$ and $O(1)$ [76], and by exploiting inter-specification correlation through vector-valued multi-task GPs in [77].

The high-dimensional problem, which confines traditional BO to roughly twenty design variables, has attracted the largest body of work: dropout with mutual-information variable selection recast in the g_m/I_D feature space [79], continuous device representations learned by variational autoencoders (VAEs) that render mixed-variable spaces amenable to real-valued GPs, BO conducted directly in a VAE-enhanced latent manifold [81].

In [82], truncated subspace sampling with gradient sketching was proposed. This method further reduces the effective sampling dimensionality down to a constant upper bound with the truncated subspace sampling technique, i,ncorporating gradients, center update steps, and prior subspace features. The authors report a speed-ups between $2-4\times$ compared to state-of-the-art sampling algorithms.

More recent publications have combined BO-based methods together with several other ML algorithms. ADO-LLM [23] marks the convergence of BO with generative models, coupling a GP-BO proposer with an in-context-learning LLM agent so that black-box exploration and domain knowledge compensate for one another's drawbacks.

A region-restriction scheme in which Monte Carlo or Voronoi tree search first isolates promising local domains before local BO is applied, presented in [83]. VTSMOC further extends this line to constrained many-objective synthesis through novel acquisitions functions that avoid the super-exponential cost of hypervolume.

In [84], a similar approach is presented where authors implement high-dimensional Monte Carlo tree search algorithm for analog circuit optimization. The method integrates the advantages of Bayesian optimization and dynamic Monte Carlo tree search to obtain feasible solution spaces through adaptive clustering, thereby reducing the search range of the Bayesian optimization algorithm and improving optimization efficiency.

A yield-driven batch BO accelerated by deep transfer learning of the underlying importance-sampling estimator is proposed in [85]. Compared with the state-of-the-art methods, the experimental results demonstrated that the

proposed method can gain a 2 – 4.6× speed-up without loss of accuracy and facilitate identification of multiple failure regions for analog circuits.

Lastly, in [86] authors propose a super additive multi-algorithm inter-working optimization framework (MARIO) for analog circuit sizing, which combines 5 optimization algorithms. In comparison to baseline optimizers for sizing over 15 circuit use cases, the proposed approach achieves more than 2.59× reduction in the number of evaluations.

2.4. Reinforcement learning based approaches

Reinforcement learning (RL) [22] has rapidly matured into a central paradigm within electronic design automation (EDA), most prominently for the analog/RF circuit sizing use cases, where its general application is performance optimization and run-time speedup.

Reinforcement learning formulates a design or control problem as sequential decision making, typically cast as a Markov decision process defined by a state space, an action space, a transition model and a scalar reward. An agent observes the current state of an environment, selects an action according to a policy, and receives in return a reward signal together with a new state; no labeled input–output pairs are supplied, so the only supervision is the delayed and often sparse feedback produced by the environment itself. The mathematical foundations of RL are detailed further in [22]. A graphical example is presented in Figure 8.

In modern deep reinforcement learning the policy and value estimates are represented by neural networks, which allows the method to operate over the high-dimensional, continuous state and action spaces that arise when, for example, device dimensions, biasing choices or connectivity decisions are treated as actions and simulated circuit performance is used as the reward.

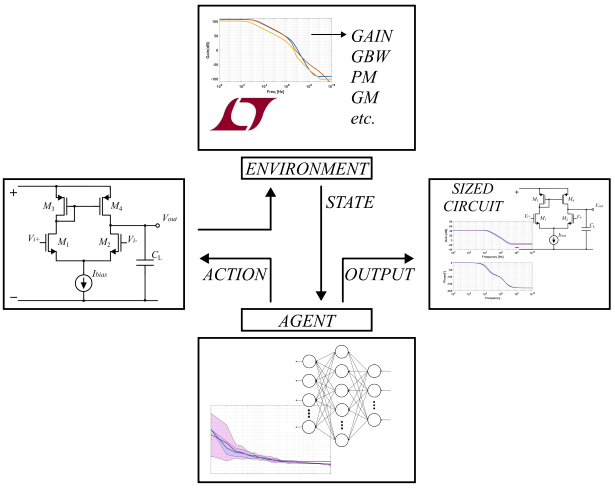


Figure 8: Reinforcement Learning optimization principle.

Early work [87] showcased promising results on different OA topologies in what regards circuit sizing. Several publications combine RL with different other ML algorithms for improved performance. In [88] and [89], authors propose a RL-GNN framework for sizing circuits. The GCN-RL agent extracts features of the topology graph whose vertices are transistors, edges are wires. Afterwards, the learning-based optimization guides the design in order to maximize the figures of merit. Both publications report favorable results for LDOs, and in [88] several OAs are the reported as use cases as well.

To tackle scalability, researchers decomposed complex circuits into sub-blocks optimized by cooperating agents for run-time reduction, as presented in [90]. In [91], a multi-agent strategy later unified across topology design and sizing OAs. The authors propose a two-task multi-agent framework with one topology design task and an optimization task each with their own set of RL agents. Compared to other publications it offers better results with the same computational resources. Lastly, in [92] authors propose a paralleled by multi-actor approach that improves figures-of-merit up to 34% compared to other state-of-the-art publications.

Other efforts target robustness and sample efficiency; several publications employ, as in previous cases, combinations of different ML algorithms in parallel in RL. In [93], a hybrid Bayesian optimization with RL is used to size OAs considering PVT-variation-tolerant sizing. In [94], authors are embed g_m/I_D methodology into sequential agents for a more stable convergence over a numerous amount of use cases, including three different OA variations and two type of continuous-time linear equalizer circuits. In [95], a similar g_m/I_D approach is undertaken but with a single RL-agent.

Beyond sizing, RL approaches to topology synthesis is reported in [96]. In [97], a comparative study against metaheuristics algorithms is done and concluded that RL agents perform better in high-complexity designs. In [98], authors introduce a multi-objective RL approach for IC optimization; the approach is tested on 4 different use cases(2 OAs, 1 Comparator ,1 LC Oscillator) and compared to other algorithms as well. The framework achieves performance that is comparable to, and in several cases slightly better than, state-of-the-art metaheuristic algorithms across all benchmark circuits.

RL-based approaches have also had success in layout routing and floor-planning [7, 8, 99] and demonstrated order-of-magnitude convergence gains over genetic algorithms while accounting for layout parasitic extraction [100].

2.5. Large Language Model aided design

The advent of large language models (LLMs) has opened new frontiers in numerous fields, demonstrating remarkable capabilities in understanding and generating complex patterns and structures. This makes LLMs particularly promising for tackling the intricate challenges of automated analog circuit design. The core strength of LLMs lies in their ability to process and synthesize vast amounts of data, learning underlying patterns and relationships. In the context of analog circuit design, this translates to the potential for LLMs to understand and generate the nuanced and often non-linear relationships between different circuit components and their performance characteristics. In re-

cent publications there is a consistent growth of LLM-aided design of integrated circuits.

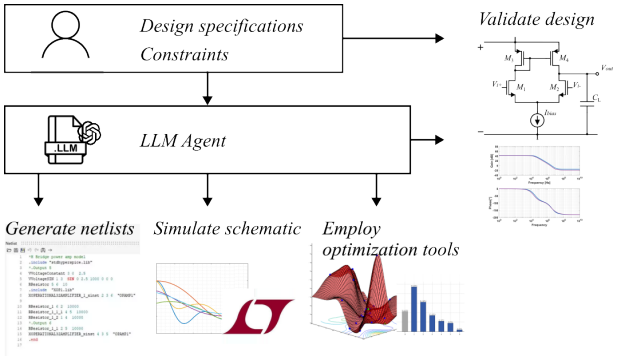


Figure 9: LLM principle.

Across this body of work, LLM-based methods have moved analog EDA from theoretical demonstrations toward measurable performance gains over previously preferred classical black-box optimizers. For circuit sizing, agentic frameworks that combine chain-of-thought reasoning with simulator-in-the-loop feedback have achieved high success rates with dramatically fewer simulations.

In [101, 102], LLM-based AI agents were proposed, capable of designing various analog and mixed-signal circuits. A similar framework, reasoning-driven multi-agent workflows, cuts simulation counts by roughly 28× relative to reinforcement-learning baselines, and was proposed in [103].

In [104], an effective framework for sizing and topology selection was presented. The LLM-based frameworks are capable of accelerating OA design by $20-50\times$ over BO- and RL-based baselines while achieving up to 90% success. An improved approach was showcased in [105]. Atelier's [105] multi-agent, knowledge-base-augmented approach delivering up to 7.89× higher figure-of-merit than Artisan [104] and 100% success across all specification sets. OAs are specifically also targeted in [106] with improvements between $13\%-48\%$ when compared to baseline approaches.

Coupling LLMs with classical optimizers has also shown clear benefit [107]. ADO-LLM met all design constraints where pure Bayesian optimization or pure LLM proposals each missed one to two specifications [23] and EasySize [108], a lightweight fine-tuned model, outperformed AutoCkt [100], a traditional RL-based optimization framework, on 87% of sizing tasks while cutting simulation resources by over 96%.

In topology generation, LaMAGIC's [24] supervised fine-tuning achieved up to 96% success under strict tolerance and more than doubled the success rate of RL search, while AnalogCoder-Pro [109] proposes a multimodal feedback loop which solved 28 of the reported 30 benchmark circuits and achieved up to 2× better OAs figures of merit than prior generative baselines. Lastly, AnalogXpert [110] proofreading-based agent quadrupled the success rate of AnalogCoder [111] on real-world topology synthesis tasks. Also, in [112] VLM-CAD was proposed, a VLM-optimized collaborative agent workflow for robust multimodal reasoning in analog circuit sizing. By integrating the neuro-symbolic parsing capabilities of Image2Net, authors successfully address the inherent spatial blindness of VLMs, anchoring their reasoning in hallucination-free topological representations. Image2Net is a structural parsing module which transforms raw pixels into explicit topological graphs and structured representations to anchor VLM interpretation in deterministic facts.

Beyond sizing and topology generation, LLMs have been applied to auxiliary EDA tasks: Schemato reached a 76% compilation success rate converting netlists to human-readable schematics [113] and ChatEDA's [25] fine-tuned AutoMage2 controller outperformed GPT-4 by 20 percentage points on RTL-to-GDSII flow automation. The versatility of LLM approaches has been demonstrate over a wide range of circuits, and further synthetized in Table 1.

3. An application perspective

Machine learning has been successfully used in applications such as circuit design optimization and verification, as well as analog layout generation. There are certain advantages when using machine learning models instead of simulated circuits that are directly related to simulation costs regarding both the simulation time and licensing costs.

In Figure 10 a general design flow is presented. Each phase has been approached by ML applications: system-level topology generation [115, 116], circuit sizing and optimization [45, 65], pre-silicon and post-silicon testing and verification [117, 118, 119] and lastly, ML-assisted automated layout [7, 8].

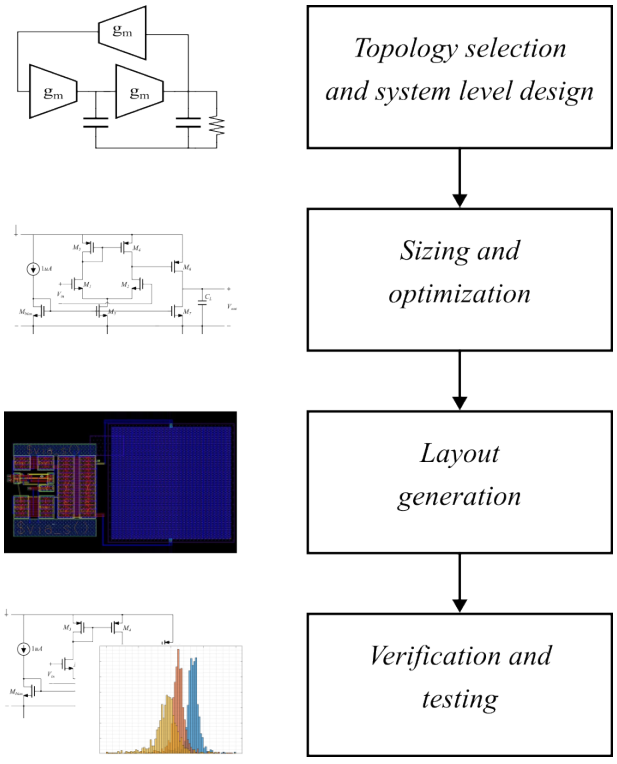


Figure 10: IC design flow.

The following subsections will be a review of state-of-the-art approaches from the perspective of applications

Table 1: Comparison between LLM-based papers for analog IC EDA published in literature.

LLM Framework	Application	Circuit Use Case	Results
EEsizer [101]	Circuit sizing, Parameter tuning	Operational Amplifiers & others	OpenAI o3 exhibited the best overall performance, achieving a 100% success rate across all circuits with the fewest iterations and the lowest variability, compared to the other tested LLMs;
AnaFlow [103]	Circuit sizing, Design-space exploration, Analog design assistant	Operational Amplifiers (two-stage Miller OA; differential folded-cascode OA with CMFB)	AnaFlow solved two-stage opamp in 9 total simulations (vs. 1035 for RL baseline AnaCraft); solved folded-cascode opamp in 64 simulations (vs. 1808 for AnaCraft), ~28× fewer simulations;
Artisan [104]	Circuit sizing, Topology selection, Automated schematic generation	Operational Amplifier (three-stage opamp)	Accelerated design process 20.4×–50.1× vs. baseline RL and BO methods; success rate up to 9/10 vs. 0–4/10 for baselines;
Atelier [105]	Circuit design automation, Topology synthesis, Parameter tuning	Operational Amplifier, Comparator	Atelier-1: 1.57×–4.70× FoM improvement and 53.8×–87.3× runtime speedup vs. black-box methods; 1.19×–2.63× FoM improvement and 2.55×–4.65× speedup vs. Artisan; Atelier-3 achieved 100% success rate across all specification sets, up to 7.89× FoM improvement over Artisanl;
EasySize [108]	Circuit sizing, Parameter tuning	Operational Amplifier	Outperformed AutoCkt [100], a baseline RL-method, on 86.67% of tasks with >96.67% reduction in simulation resources;
AnalogXpert [110]	Circuit topology generation	General Analog IC Design	40% success rate (synthetic dataset) and 23% (real dataset), vs. GPT-4o (3%, 3%) and AnalogCoder [111] (8%, 6%)
AnalogCoder-Pro [109]	Circuit topology generation, Circuit sizing, Circuit design automation	General Analog IC Design	Successfully designed 28/30 benchmark circuits; up to 2× better OA FoM vs. AnalogGenie [114]
Schemato [113]	Hardware description generation (netlist-to-schematic conversion)	General Analog IC Design	76% compilation success rate vs. 63% for best baseline LLM; 1.8× higher graph-edit-distance score and 4.3× higher MSSIM (scaled by CSR) than best pretrained models
ADO-LLM [23]	Circuit sizing, Design-space exploration	Operational Amplifier (two-stage differential amplifier), Comparator (hysteresis comparator)	FoM of ADO-LLM 3.52 (OA) with 0 missed specs, vs. GP-BO (1.89–2.10) and LLM-only (0.20) with 1–2 missed specs;
LaMAGIC [24]	Circuit topology generation	DC-DC Converter (Power Converter)	Achieved up to 96% success rate under strict 0.01 tolerance; outperformed RL-search baseline (0.41 success rate) by more than 2×; up to 37.5% higher success rate and 58.5% lower MSE;
ChatEDA [25]	EDA automation, Design automation (RTL-to-GDSII flow)	General Circuit Design (digital, not analog-specific)	AutoMage2 achieved 82% Grade A on ChatEDA-Bench vs. GPT-4's 62% Grade A

used in order to automate various phases of the development flow. Firstly, the circuit sizing, optimization and recent developments in topology generation will be addressed and afterwards other phases of the analog integrated circuit design cycle that found great success with machine learning applications will be briefly discussed.

3.1. Circuit sizing and optimization

The problem of sizing (or sizing-tools) is rather straightforward, given that a simulation database is pre-existent, or, if there are no issues with what regard time and economic expenses, uniformly sampling our search space and densely enough could lead to good results, as presented in [31] and [120]. The optimization problem is more sophisticated given that a pre-existent database isn't available a more careful or intelligent approach is needed. In this sense, several optimization algorithms can be used to achieve the desired results. Promising results have been obtained with RL [93, 89], BO [75], EA [3, 73] and ANNs [30, 31].

In most publications which present machine learning models that predict circuit behavior the acquisition process for the training data is rarely discussed. They are commonly obtained by either randomly or uniformly sampling the desired search space. In [121] and [53] authors propose an adaptive sampling method of developing these models by optimizing the acquisition process such that the best model is obtained with the least amount of sample points. By optimizing the number of samples an improvement is obtained which afterwards results in lower use of expensive simulations which is the case with finite element analysis simulators.

Circuit sizing, implies a machine learning regression model that is used for predicting certain performances. When talking about circuit optimization, it is often the

case that some design specifications are needed to be either maximized or minimized and are usually difficult to obtain through hand design, and some machine learning algorithm might be of help in this area. In some cases, a circuit sizing model might be coupled with an optimization algorithm for some particular applications instead of using the commercial tools available for simulations.

Table 2 comprises a list of publications which used circuit sizing and/or optimization, as well as the samples used or accuracy where it is reported. Algorithm-wise, for various sizing problems artificial neural networks seem to be the preferred machine learning algorithm [1, 2, 29, 33, 37, 44, 46], some reasons could be the ease of implementation, robustness and scalability with bigger data sets. For the circuit design optimization case a considerable amount of implementations are done using Bayesian optimization [74, 75, 77, 93, 122] and also notable reports with evolutionary algorithms [4, 45, 57, 60, 73].

Figure 11 shows the general method for developing a machine learning model that can predict outcome of simulations parameters. For a set of performances (i.e. Phase margin, Gain margin, PSRR, CMRR, Slew-rate, etc.) the machine learning algorithm should be able to provide the physical parameters of our components: widths and lengths of transistors, reference currents and voltages and compensation resistance and capacitance.

Table 2: Comparison between papers published in literature.

Ref.	Task	Samples/Accuracy
[2]	Sizing	5000/ –
[1]	Sizing	120000/–
[33]	Sizing	150000 / –
[29]	Sizing	20000/92%
[44]	Sizing	–/>95%
[123]	Sizing	13500 / >90%
[124]	Sizing	– / –
[3]	Optimization	– / –
[4]	Optimization	2000-15000 / -
[45]	Optimization	10000 / >80%
[32]	Optimization	1900000 / >95%
[89]	Optimization	20000 / –
[125]	Optimization	– / –
[122]	Optimization	300-3000 / –
[46]	Sizing & Optimization	– />95%

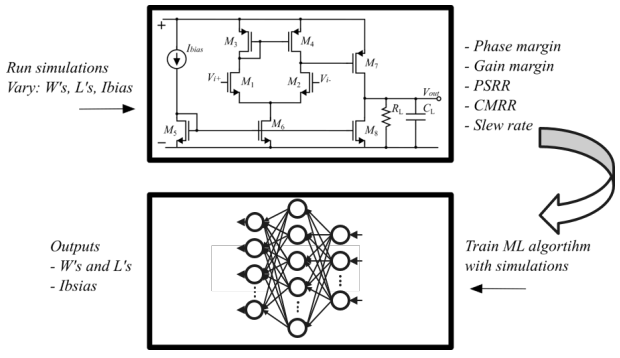


Figure 11: Neural networks based parameter prediction

In a first step, simulations are run by varying the circuit parameters (widths, lengths, resistances, etc.) either randomly or uniformly or by any procedure the application designer seems fit and afterwards by getting input-output simulation points a machine learning regression algorithm can be trained which can accurately predict based on design specification (gain margin, phase margin, etc.) the corresponding design parameters. Further simulations can be performed if the model is not at the expected accuracy, making sure not to duplicate or overlap samples, but this in practice might become difficult and resource consuming for large data sets.

In [29, 33, 37, 44, 46] the implementation was done via artificial neural networks. The neural network is trained with prior obtained simulations varying the circuit parameters (P) which can represent W's, L's, resistances, capacitances, etc. They are commonly varied either by grid, uniformly or randomly. Based on the training data and assuming a good enough model was obtained it can be further used to predict new design with set design parameters (DP). As previously discussed ANN-based reports has been implemented with robust results in [29, 37, 44] reaching overall accuracy of up to 95%. Regarding ANN use it is not mandatory to group all outputs in one network, another option being to develop a model for each circuit parameter and based only on a partial set of design parameters which are of interest or they are known to be highly correlated from prior data [53].

In [126], the authors propose a two-step method that takes advantage of behavioral synthesis that is capable of fast and broader coverage of the design space, then makes correction on sizing, refining by SPICE simulation.

Figure 12 presents the general framework for a circuit optimization methodology, usually a machine learning optimization framework is used, such as Bayesian optimization or reinforcement learning, in a loop with a simulation environment (which can as well be modeled by previously mentioned machine learning models) and based on the circuit responses, the machine learning algorithm chooses the next simulation point to be explored until the objective is met or the simulation budget is reached.

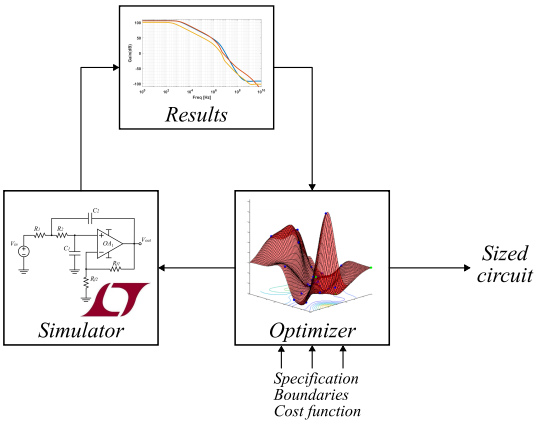


Figure 12: Simulator-in-the-loop optimization

In Figure 13 an ML-in-the-loop alternative is presented.

The advantage of using a machine learning model as a placeholder for the simulation environment is that the response is practically instantaneous (in the order of milliseconds) and no additional simulation effort is required than the initial simulations for developing the model.

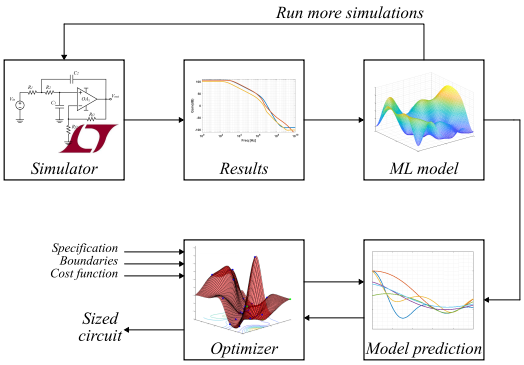


Figure 13: Metamodel-in-the-loop optimization

The machine learning model can be reused in other phases of the development cycles as well for further projects which use the modeled circuit, bringing further benefit to the approach. In [127], a similar approach is attempted, by building precision response surface models for different outputs of an low dropout regulator, which subsequently were used in optimization of PSRR and temperature coefficient (TC).

The utility of machine learning algorithms for circuit sizing and optimization has been shown to produce high-quality designs given a certain set of design specifications. However, current state-of-the-art methods cannot replace human experts in the analog design flow. The main challenge is that the models learn from a limited data set, thus having limited flexibility. Current research trains and tests its algorithms on a few classes of circuits, each having a very narrow application space, a generalized model designed for a variety of circuits might be an interesting area of study. Another potential bottleneck is the vast space of system-level design, which the presented machine learning approaches have not yet exploited but may be applied to in the future.

3.2. Topology optimization of integrated circuits

The earliest and most persistent line of work casts topology generation as an evolutionary search over device-level structure. In [63], the authors propose a framework which evolves comparator topologies from elementary building blocks with a genetic algorithm. In [67], device-level synthesis is proposed: variable-length chromosomes encode arbitrary transistor-level connectivity, and topology and sizing co-evolve from scratch without predefined templates, with adaptive acceptance, redundant-component removal, and segmented evolution improving robustness. The paper reports several fully functional amplifier designs.

Two further frameworks are better described as topology selection than as topology generation, but remain relevant to the connectivity-decision stage. In [128], the author selects from a modular, parameterized library, using a variational autoencoder to augment the topology dataset with synthetic data before an ML predictor picks and re–sizes the optimal candidate. In [50], the authors couples topology selection with sizing through a semi-supervised co-learning scheme, in which neural networks infer the behavior of complex topologies by composing simpler ones,, and thereby cutting labeled-data requirements.

More recent evolutionary methods act not on raw netlists but on learned representations. In [116], the authors converts behavioral OA graphs into a performance-aware embedding via a GNN trained for performance prediction, then runs a genetic algorithm over that representation with a surrogate model, coupling the search directly to the downstream performance objective. In [129], the authors optimizes over a learned latent space but structures its encoder as a two-level nested GNN that represents circuits as combinations of subgraphs from a known basis, jointly yielding topology and sizing.

In [130], a generative adversarial network is trained to map a low-dimensional latent space to circuit topologies, using the discriminator to improve generator quality and thereby reaching synthesis problems too large for enumeration. In [114], authors propose an LLM-based approach, which is capable of discovering unseen structures and larger device counts than prior art.

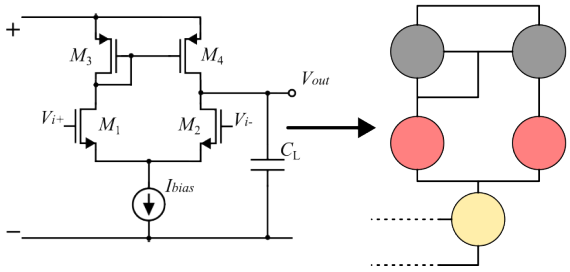


Figure 14: Graph example reproduced from [88].

The most recent shift reframes topology generation as program or netlist synthesis performed by large language models embedded in agentic loops. In [110], the authors formulates the task as subcircuit-level SPICE code generation and injects design expertise through a proofreading strategy that incrementally corrects an initial design. In [105], the authors distributes the work across specialized LLM agents arranged in a graph-of-thoughts structure – with distinct topology-selection and topology-modification agents – that consult a compact knowledge base and use self-reflection and backtracking to refine connectivity.

Regarding the use case for which the mentioned techniques were applied, most of the publications report various OA use cases, with one paper reports a comparator as an use case which we can consider a sub-class of OAs, with later reported results with LLMs tackle more than one circuit use case [105, 109, 110]. This suggest that topology generation/selection is still in an incipient phase.

3.3. Circuit verification

The purpose of verification is to ensure that the design of the integrated circuit meets the requirements and

prevents faulty integrated circuits from spilling into the market or customer base. During the development cycle, the chips are subject to multiple testing phases. We can identify two main distinct categories, namely pre-silicon and post-silicon verification [131]. The former phase refers to the tests performed tests before the chip is manufactured mainly concerned with the functionality of the circuit in different operating conditions, regarding process, voltage and temperature. The latter involves evaluation of the manufactured chip, detect structure defects and certifying correct behavior within the specified domain.

The first phase of the verification process (i.e. pre-silicon verification) is run during the design stage. The process tries to validate the design guaranteeing there are no design faults and that circuit works properly. This usually relies on heavy simulator use for coverage of all the test scenarios. Consequently, low coverage in simulation leads to functional defects in the design that spill into production, eventually reaching the delivered products. This makes the pre-silicon verification phase an essential part of the design cycle; the design does not go through any further development if it doesn't pass the verification process successfully [132].

With the recent advances in machine learning, various research papers proposed approaches to hand complex problems in both areas of pre-silicon and post-silicon verification [6, 5, 133, 134, 135, 136, 137, 138, 139]. One such topic is pre-silicon hotspot detection, conventional approaches widely rely on full chip lithography simulation [133], this being computationally expensive.

Several approaches that aim to speed up the verification process have been reported [133, 134, 135, 136, 137, 138] with different algorithms such as support vector machine (SVM) and ANNs, both offering good results in this aspect.

Another area that had great benefit from machine learning approaches is process-voltage-temperature (PVT) variation. Atypical approach to designing for pre-silicon variation is a Monte Carlo grid, which is usually done through a grid in the voltage-temperature space and Monte Carlo sampling of the process space [6, 5, 139].

The main limitations of this classical approach can be the low coverage in the voltage-temperature space and the high number of required simulations. In this direction and with the aim of reducing some of the limitations of the Monte Carlo grid traditional method, optimization methods and algorithms were used, such as: Bayesian optimization or Genetic algorithms. These algorithms can reduce the number of simulations; nevertheless, they have several limitations: high computational costs and even the need to tune a large number of hyperparameters, which can bring high costs, in terms of resources [5, 6, 139].

3.4. Machine Learning for Automated Analog Layout

Naturally, after the schematic design fits into all design specifications the layout phase is started. Thus, tools that help with automatic analog layout [7, 8] are an attractive topic for a lot of researchers, hence research publications started to appear. In this sense, a short summary of recent publications regarding problems that have been addressed with electronic design automation approaches is discussed in the following paragraphs.

Pre-layout and post-layout simulation can differ greatly because of the problem of parasitic elements. The implementation is based on state-of-the-art graph neural networks [140] used to model electrical simulation errors based on large industrial circuit data sets.

The routing of analog integrated circuits is addressed in [141] authors develop GeniusRoute, a framework that automatically extracts routing regions from human layouts and applies the acquired knowledge into the analog router tool. They report performances close to manual design and a state-of-the-art implementation outperforming previous analog routing approaches. In [142], WellGAN uses a generative adversarial network to propose well-guiding regions, followed by a rule-based validation stage, yielding wells close to manual designs with comparable post-layout circuit performance.

ParaGraph [143] converts schematics into graphs and predicts net parasitics and layout-dependent device parameters. GANA [144] applies a graph convolutional network to hierarchical subcircuit recognition, which extracts the symmetry and matches constraints that hierarchical layout requires, with accuracy reported qualitatively across OTAs, LNAs, mixers, oscillators and filters.

Some progress has been made with placement and floor planning as well. In [145], the authors compare a neural network, random forest and SVM based analog IC placement tools; the neural network attains 88.7%, SVM attains 78.4% and random forest attains 76.2% classification accuracy. Simulation results from several amplifier designs indicate that the proposed approach can achieve performance similar to manual layout but is orders of magnitude faster. In [146], a deep learning approach is proposed for placement optimization. A case-study comparison with a floorplan design made by a human-expert is presented, and improvements in the fulfillment of every constraint, reaching an overall improvement of around 70%, demonstrating the approach's value in placement design.

4. A circuit use case perspective

Lastly, a review of literature regarding use case is performed. This aspect is also important to put into perspective what is achievable regarding different circuit classes, either in modeling, optimization, or other phases of the analog design cycle. From Figure 15 it is easily observable that operational amplifiers (OAs) are frequently used as test use cases since they are fundamental building blocks present in almost all analog circuits. With most of applications being performed on OAs followed by consecrated types of circuits, namely voltage regulators and oscillators which will also analyzed in further subsections. Subsequently, more complex circuits often contain the aforementioned circuits, thus performing optimizations on such lower-complexity circuit might facilitate their usage in more complex systems.

Few publications report several classes of circuits, mainly due to their complexity both in behavior and in modeling. ADC/DACs are mentioned in very few publications, because they are complex systems that bridge between the

analog and digital fields, and also contain several blocks which have been optimized in prior publications, such as oscillators, comparators and and operational amplifiers. Another class of circuits which are rarely discussed in EDA topics are DC/DC converters, or more generally, switching circuits, which have recently been discussed in [24] as a novel class of circuits.

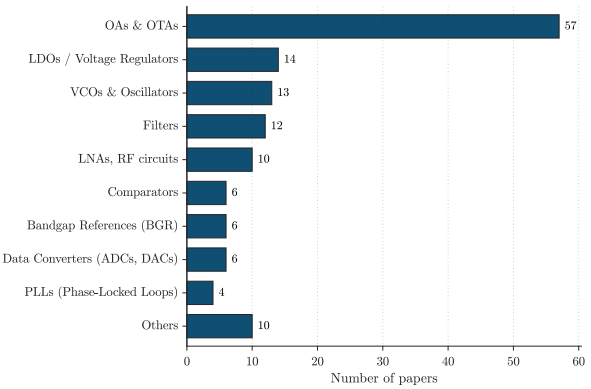


Figure 15: Frequency of different circuits reported in literature as use cases.

4.1. Operational amplifiers

OAs come in various forms such as single-stage, two-stage and three-stage or multi-stage amplifiers, with the two-stage operational amplifier being the cornerstone of most applications, and also being the most utilized use case. As can be seen in the graph from Figure 16.

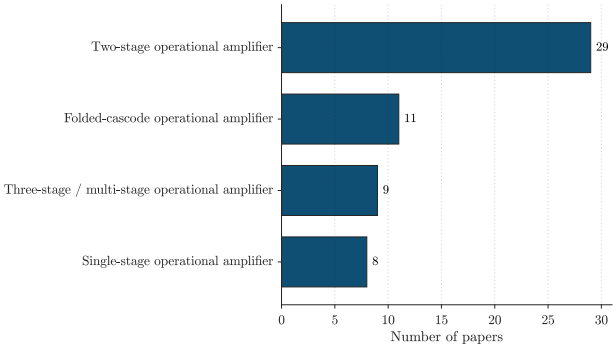


Figure 16: Frequency of different types of OAs reported in literature as use cases.

The literature report several ML applications with this type of use case, raging from sizing tools, which are able to predict both performances based on design parameters and vice-versa, as discussed previously. The two-stage Miller OA is the most popular use case. Subsequently, the OA has been also a typical use case in several optimization frameworks [46, 57]. Lastly, analog layout applications have also utilized several versions of OAs as use cases [142, 143]. In [147], an exhaustive approach was proposed which automatically generates OAs from specification to layout.

In [148], a comparison for the number of simulations used in the development of machine learning models for the Miller OAs use case is presented with numbers up to 10000 simulations reported to size a circuit, other reports [2, 75, 122] give numbers between 500 and 5000 points for either modeling ,with reasonable accuracy, or optimizing a predefined topology. A few publications report higher numbers between 50000 and 150000 samples used in developing the machine learning models [1, 33, 46]. This number is dependent on the number of parameters used but gives us a rough estimate of the number of simulation points needed. If this is the case, the development of machine learning models that can be used as a placeholder is done with fewer simulation points, such that a speed-up in the development process is obtained by reducing both simulation time and cost.

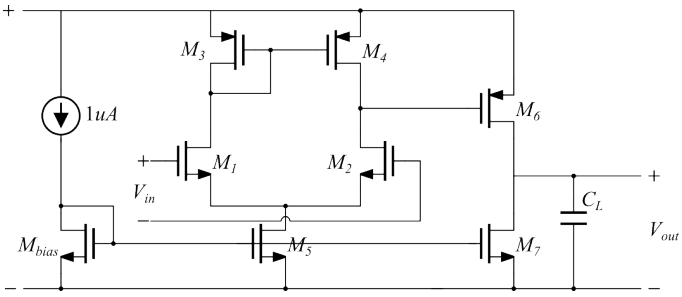


Figure 17: Topology of a two-stage operational amplifier.

In Table 3 a comparison of several similar three-stage OAs is presented. For all the reported figure of merits (FoMs) the same formula was used which is presented in equation (10).

$$FoM = \frac{GBW \cdot C_L[pF]}{Power[mW]} \tag{10}$$

Table 3: Reported performances obtained for similar three-stage operational amplifiers reported in literature

Reference	FoM	Specs
[116]	503.000	Gain= 89 dB, GBW=2.39 MHz, PM=56°, Power=47 μW
[91]	560.038	Gain=99.3 dB, GBW=2.5 MHz, PM=57.7°, Power=44.7 μW
[115]	333.998	Gain= 86 dB, GBW=1.8 MHz, PM=57°, Power=88 μW
[149]	356.560	Gain=106 dB, GBW=1.62 MHz, PM=62°, Power=45 μW
[150]	368.131	Gain= 87 dB, GBW=3.38 MHz, PM=43°, Power=91 μW

This strongly suggest that EDA Tools are capable of aiding human designers in speeding up the design process, obtaining comparable results with improvements in what regards development time. Regarding topology generation of OAs (or more general amplifiers) several approaches have been presented in the literature. Firstly, several results have been published regarding behavioral/system-level topology synthesis [116, 149]. In this type of application, OAs are generated at the system level, where authors employ a behavior-level abstraction that represents an amplification stage with a voltage-controlled current source (g_m stage),

capacitors, resistors, or other components/sub-blocks. In [116], an experimental results demonstrate that the proposed approach outperforms state-of-the-art methods in terms of both optimization efficiency and results.

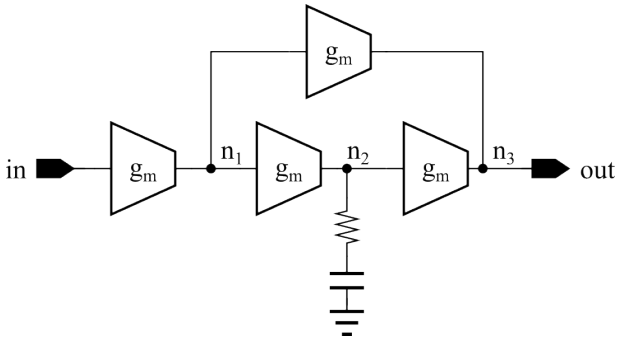


Figure 18: System level OA [116]

In [96], the authors propose a novel graph-based circuit topology refinement scheme which generates frequency compensation circuits for OAs. Compared with the state-of-the-art approaches, the proposed method boosts the synthesis efficiency by at least 3× times but also enhances the synthesis capability with a deterministic compensation scheme. A genetic algorithm approach is presented in [67] where the author propose a framework which is capable of accomplishing circuit synthesis without any prior knowledge of previously defined topologies.

Lastly, LLM-based approaches have yielded some promising results in what regards topology synthesis [110].

4.2. Low dropout regulators

Low-Dropout (LDO) regulators are essential because they provide clean, stable, and low-noise supply voltages by efficiently stepping down higher input voltages even when the input-to-output voltage difference is very small, which is critical for protecting sensitive analog circuits, preventing jitter in oscillators, and maximizing battery life in portable devices. A general topology for LDOs is shown in Figure 19.

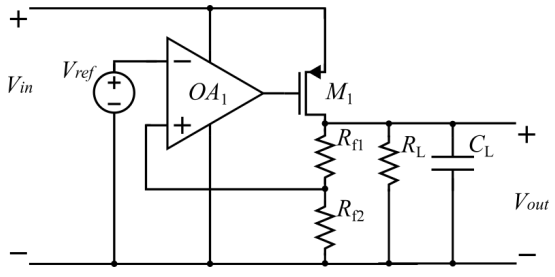


Figure 19: General topology for a low dropout regulator.

Several attempts have been made to model the behavior of LDOs in [121] and [53] with both NNs and GPRs showing favorable results for the outputs measured. In [64], a ML-based design was compared to the results obtained by a human designer, concluding that ML design tools provide stable and robust design that can speed up the engineering process. In [79], a novel BO-based approach was used, which obtained better results than other reported state-of-the-art publications.

For pre-silicon verification of circuit performance and [5, 6] propose novel techniques which can overcome the traditional corner-based PVT verification limitations, in what regards variable coverage, as well as in [139] for worst-case identification.

An interesting approach which has a high degree of novelty is [151] where the authors proposed a co-design approach for VCOs and LDOs in order to address the trade-offs between high-frequency and LDO-induced low-frequency phase noise. Simulations show that the co-design method improves phase noise by 1.2 dB at a 1 MHz offset and reduces dynamic power consumption by 28.8%, with the FoM increased by 2.4 dBc/Hz compared to the conventional sequential design method.

RL-based approaches have found success in LDO design as well. In [89], a RL framework was used together with a GNN in order to design and optimize several performance metrics such as PSRR, PM, power consumption and output ripple, with better results than other reported implementations present in the paper.

4.3. Oscillators

Oscillators, are an important class of circuits which are present in various forms in PLLs, ADC/DACs, DC/DC converters and switching circuits. The need for precise oscillations is needed to prevent timing jitter, minimize phase noise, and ensure high-fidelity signal conversion or efficient power regulation across ADCs, DACs, and DC-DC converters. In this use case we identify two distinct popular use cases, the first one are ring oscillators (commonly made by cascading several inverter stages) which are shown in Figure 20 and Figure 21 and the second one being LC oscillators, shown in Figure 22.

For ring oscillators, in [40] an ANN regression modeling technique with variational auto-encoders is proposed. The authors report good results for various technologies, achieving twice the accuracy of conventional approaches. In [152], a device modeling method for ring oscillator which considers multiple process variability source effects, was proposed. The modeling was done using an ANN-based framework which is capable of predicting both global and local variability of parameters. In [153], a parasitic-aware design optimization of a ring oscillator is proposed.

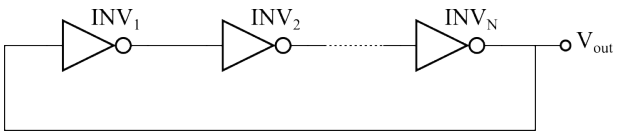


Figure 20: Topology of a ring oscillator.

In [98], an ANN-based RL framework is proposed; one of the use cases is an LC Oscillator. An automatic simulation-based approach was presented in [38]. The authors propose two distinct models, one for classifying the convergence of the design in nominal and PVT corners and a second model which predicts the oscillating

frequency of the design. Overall, they report a 19% reduction in simulator use. In [120], both ring-oscillator and a LC-VCO were modeled with considerably good results using several sampling techniques. In [65], an evolutionary algorithm-based approach is proposed for optimizing VCO performances when trade-off are considered. Lastly, in [44] a cascaded ANN framework is proposed for sizing various RF circuits (with VCO example as well) obtaining an error of less than 5% across all the tested use cases.

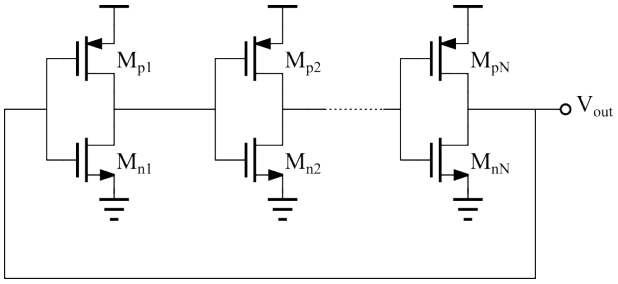


Figure 21: Topology of a ring oscillator- transistor level.

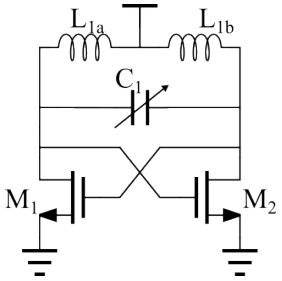


Figure 22: Topology of a general LC voltage controller oscillator.

5. Conclusions

This survey has examined how machine learning and metaheuristic optimization are being applied to the automation of analog integrated circuit design. The scope was deliberately restricted to the analog domain; the characteristics that have historically resisted automation in analog design – strong device non-linearity, continuous and interdependent design variables, high sensitivity to process, voltage, and temperature variation, and specification spaces with partially conflicting objectives must be satisfied simultaneously.

Sizing of a fixed topology remains overwhelmingly the dominant task, various algorithm have been shown to be capable of delivering robust and reliable designs. Topology synthesis is the fastest-growing sub-field, but it is also the one in which evaluation is weakest, since a generated netlist is considerably harder to score than a sized one.

Several limitations recur throughout the literature and should be read as the principal obstacles to further progress. First, benchmarking is fragmented: results are reported on private circuits in undisclosed technologies, and cross-paper comparison is therefore largely difficult to assess; recent open benchmark suites are a necessary corrective but are not yet widely adopted.

The mapping between algorithm families and design tasks is by now reasonably clear. Evolutionary algorithms remain a popular choice for analog sizing, valued for their tolerance of discontinuous, constraint-heavy search spaces, and they have proved the most natural host for topology-level representations. Bayesian optimization has become the method of choice wherever the simulation budget, is the binding constraint. Large language models are the newest entry and the fastest-growing, and they are the only family offering a route from natural-language specification to netlist; they are also, at present, the least rigorously validated. Across all families, the most productive recent work is hybrid: surrogate-assisted evolutionary search, graph-based policies embedded in reinforcement learning loops, and language models used as topology proposers with classical optimizers as the sizing back end.

The direction of research is nonetheless clear. The field is converging on unified flows in which topology selection, sizing and layout are optimized jointly rather than sequentially, on foundation-model-style circuit representations that can be reused across tasks, and on shared benchmarks that render comparative claims meaningful. Whether analog design automation attains the maturity long enjoyed by its digital counterpart will depend less on the invention of new algorithms than on the discipline of evaluation applied to those already available.

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